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Probing the Surface Glass Transition Temperature of Polymer Films via Organic Semiconductor Growth Mode, Microstructure, and Thin-Film Transistor Response

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Abstract: Organic semiconductor-based thin-film transistors (TFTs) have been extensively studied for organic electronics. In this study, we report on the influence of the polymer gate dielectric viscoelastic properties on overlying organic semiconductor film growth, film microstructure, and TFT response. From the knowledge that nanoscopically-confined thin polymer films exhibit glass-transition temperatures that deviate substantially from those of the corresponding bulk materials, we show here that pentacene (p-channel) and cyanoperylene (n-channel) films grown on polymeric gate dielectrics at temperatures well-below their bulk glass transition temperatures [T_g(b)] exhibit morphological/microstructural transitions and dramatic OTFT performance discontinuities at well-defined temperatures [associated with a polymer "surface glass transition temperature," or T_g(s)]. These transitions are characteristic of the particular polymer architecture and independent of film thickness or overall film cooperative chain dynamics. Our results demonstrate that TFT measurements represent a new and sensitive methodology to probe polymer surface viscoelastic properties.

Introduction

The glass transition temperature, T_g, of amorphous polymers is considered to be one of the most important parameters for describing fundamental viscoelastic properties, as well as for targeting technological applications.[1−3] At temperatures above T_g, amorphous macromolecular materials are rubbery, viscous fluids, while below T_g, they are described as glassy and more or less brittle.[4−6] Several studies have investigated to what degree the surface and interfacial T_g's of polymeric materials vary vs the bulk values, with the motivation being their important role in diverse applications such as photoresists, disk drive lubricants, membranes, nanocomposites, and biomaterials.[7−9] To design highly functionalized polymeric materials, understanding the physical properties in the vicinity of the film surface and critical interfacial regions, which are impossible to deduce via simple extrapolation of bulk parameters, is of great significance.[10]

Nanoconfined polymeric glass-formers exhibit T_g's that deviate substantially from their bulk values. Due to the ease of confining film dimensions and varying thickness, thin polymer films have been heavily studied to understand their nanoconfined macromolecular behavior.[11] For polymer films supported by a substrate, as the film thickness decreases, T_g increases for polymers with strong attractive substrate interactions such as hydrogen bonding[12−18] and decreases for polymers with neutral or repulsive substrate interactions (Figure 1).[12−15,17,19−29] Many

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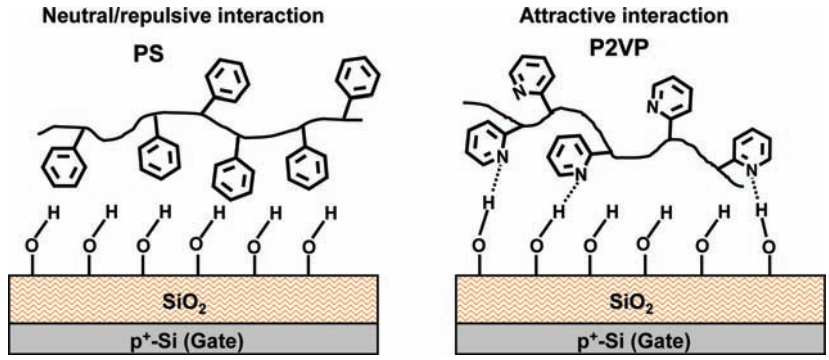

Figure 1. Schematic representation of polymer films having neutral/repulsive (left) and attractive (right) substrate interactions on SiO_2 substrates. Polystyrene (PS) and poly(2-vinylpyridine) (P2VP) are used as representative polymers for these categories.

studies[12,13,24,30−32] indicate that free surface and interfacial effects are the most logical explanations for the underlying origin of these T_g deviations. Polymer segments at the free surface experience fewer conformational restrictions than those in the bulk and thus have higher degrees of cooperative segmental mobility and lower T_g values, while polymer segments at interfaces having strong attractive substrate interactions experience lower degrees of conformational freedom and exhibit elevated T_g values. Furthermore, it has been observed that the region of anomalous T_g at the free surface or interface with the substrate is not locally confined but persists several tens of nanometers into the film interior with a continuous distribution.[28] Various experimental techniques have been employed to measure T_g in polymer films, including ellipsometry,[13−15,19,22−27] dielectric relaxation spectroscopy,[21,33,34] fluorescence spectroscopy,[17,28,35−40] Brillouin scattering,[27,41] X-ray reflectivity,[16,29] and nonlinear optics.[42] Note that all of these spectroscopic methods measure essentially the "average" T_g across the polymer film for all accessible thicknesses. Possibly for this reason, T_g depression at free polymer surfaces has never, to our knowledge, been probed directly before our recent communication describing its effects on organic thin-film transistor performance,[43] and no studies have reported reduced T_g values in polymer films having attractive substrate interactions such as poly(2-vinylpyridine) (P2VP) or poly(methyl methacrylate) (PMMA) on silica or glass substrates.[14−17,44]

The thin-film transistor (TFT) is the central device structure of all modern electronics. It can be used as a switch or an amplifier and can be straightforwardly implemented as a testbed for evaluating the semiconducting properties of organic and inorganic materials.[45] A TFT is composed of three essential components—semiconductor, dielectric, and conductor (gate, source, and drain; Figure 2), and the electrical current is controlled by application of the gate field. The function of the dielectric is to accumulate/stabilize carriers (holes or electrons) at the semiconductor-dielectric interface and to suppress leakage of current between the semiconductor and the gate electrode. To have efficient, durable, reliable electronics, each TFT device component must perform its role at an optimum level. To this end, for the past 50 years, TFTs fabricated from inorganic materials such as silicon as the semiconductor, silicon dioxide as the insulator, and metals such as aluminum and copper as the conductors, have dominated electronics.[46] However, these inorganic materials have limitations which will restrict many future applications as a consequence of their mechanical fragility, optical opacity, small achievable areas, high production costs, and incompatibility with low processing temperatures and reel-to-reel manufacture.

Given the limitations of conventional inorganic material-based TFTs, the unique characteristics of organic materials offer great promise in numerous applications. Beginning three decades ago with the discovery that organic molecular materials can function as electrical conductors, this field of '*organic electronics*' is now on the verge of the first large-scale commercial applications. Facile tuning of structure over many length scales, low-cost high throughput manufacturing methods by printing as one prints a newspaper or a magazine, and compatibility with flexible substrates are some of the exciting features of contemporary organic electronics. To this end, organic TFTs (OTFTs) have gained considerable attention as the enabling component of inexpensive/disposable "printed" electronics such as RF-ID tags, flexible displays, and sensors.[47−52]

Given the promise of organic molecules as TFT components, there have been intense efforts to develop and optimize new

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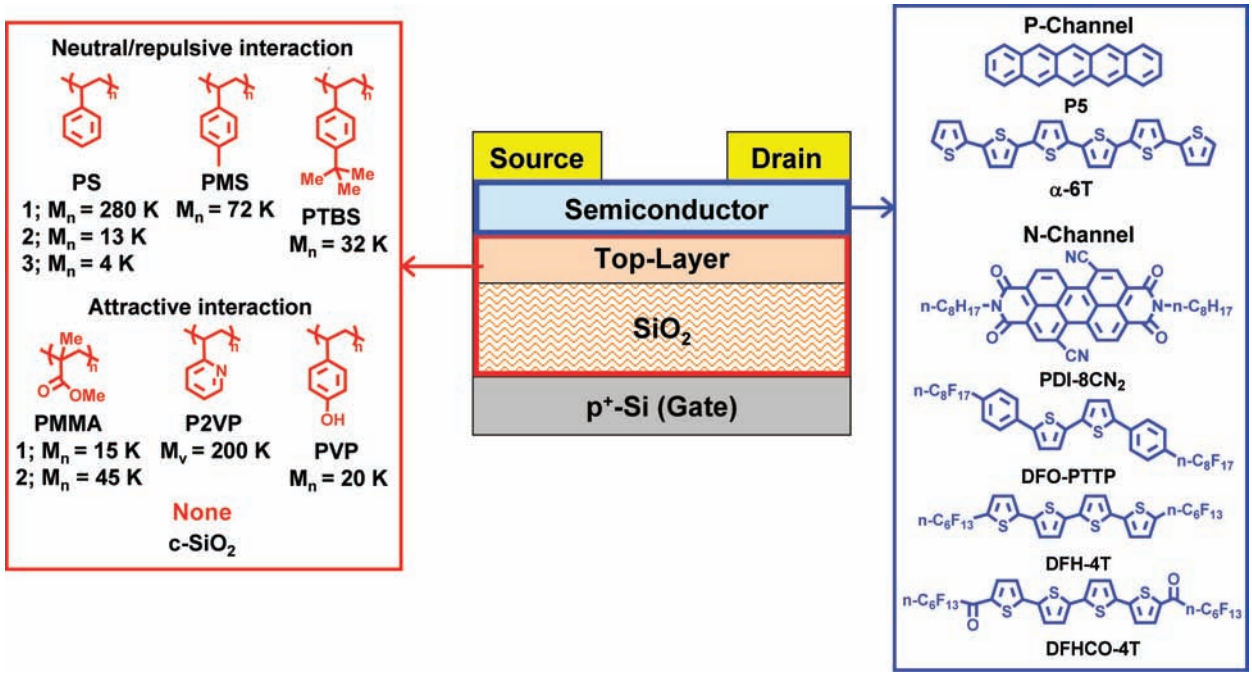

Figure 2. Schematic representation of the top-contact/bottom-gate OTFT structure and the polymer/semiconductor structures employed in this study.

organic-based materials as semiconductors, dielectrics, and conductors. Because of substantial recent progress in organic semiconductor performance, carrier mobilities comparable to or surpassing those of many common inorganic semiconductors have now been demonstrated.[45] At the same time, organic gate dielectrics require further development to enhance performance and to understand how organic insulator properties affect overall TFT response. Since OTFT charge transport is confined to very a thin (a few monolayers) semiconductor layer at the semiconductor/dielectric interface, several studies have addressed the manipulation/understanding of the semiconductor/dielectric interface to enhance device performance.[53−58] To this end, polymeric gate dielectrics are ideal candidates due to ease of processing and diverse surface physicochemical properties.[59−65] However, the degree to which polymer dielectric chain segmental dynamics might influence organic semiconductor growth and resulting OTFT performance, as well as whether there are differences among various polymer dielectric architectures and their semiconductor or substrate interactions, have remained largely unexplored.[43]

We recently communicated that pentacene thin-film transistor performance can be an excellent probe of polymer film surface T_g [defined as T_g(s)] on the basis of the alteration of pentacene film growth mode, microstructure, and the resulting OTFT response.[43] Here we report a detailed investigation of how TFT performance can characterize the surface T_g's of polymer films used as OTFT gate dielectrics. To investigate the degree to which TFT performance alterations are solely a function of surface viscoelasticity, the polymer gate dielectrics employed in this study span a variety of architectures, from macromolecules having neutral or repulsive substrate interactions (e.g., polystyrene) to polymers having attractive substrate interactions (e.g., P2VP or PMMA), as well as having different molecular masses and other physicochemical properties (Figures 1−2 and Table 1). Furthermore, other polymer geometries such as multilayers, oxygen-plasma treated surfaces, and plasticizer-doped polymer films are investigated here to broaden scope of the inquiry. Polymer films of various thicknesses are prepared on identical 300-nm-thick thermal oxide SiO_2/Si substrates, allowing direct comparison of polymer surface viscoelastic properties under conditions of negligible gate leakage current

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Table 1. Carrier Mobility Data (μ_{sat}, $cm^2/V \cdot s$)[a] for Pentacene TFTs Fabricated on Various Polymer/SiO_2 Gate Dielectrics and on SiO_2 as a Function of Pentacene Film Deposition Temperature (T_D)[b]

gate diel.	T_g[c] (°C)	d (nm)	T_D (°C) 25	35	40	45	50	55	60	65	70	75	80	85	90
c-SiO_2	–		0.23				0.20		0.22		0.20		0.18		0.24
PS1	103	20	0.65				0.68	0.66	0.42	0.05	0.05	0.02	0.01		
		150					0.65	0.59	0.40	0.10	0.05				
		400					0.67	0.59	0.44	0.10	0.06				
		800[d]					0.68	0.57	0.38	0.10	0.08				
PS2	94	24	0.54		0.47	0.45	0.34	0.04	0.05	0.007	0.004				
PS3	83	10	0.32	0.18	0.08	0.006	0.004	0.006	5×10^{-7}						
		50	0.34	0.17	0.20	0.02	0.04	0.005	0.003						
PMS	107	20	0.73				0.63	0.65	0.58	0.56	0.25	0.15	3×10^{-5}		
PTBS	137	30	0.59							0.63	0.49	0.07–0.17	0.001–0.27	0.04–0.22	0.04
PMMA1	86	10	0.15				0.14	0.14 0	16 0	16 0	15 0	12 0	008	0.001	
		20	0.18				0.14	0.14	0.14	0.17	0.16	0.16	0.06	0.005	2×10^{-6}
		100	0.17				0.15	0.15	0.15	0.16	0.17	0.10	0.008	0.004	2×10^{-7}
P2VP	103	8	0.08				0.09	0.08	0.08	0.02	0.02	5×10^{-4}	4×10^{-6}		
		12	0.07				0.07	0.08	0.06	0.01	0.01	5×10^{-4}	2×10^{-6}		
		70	0.08				0.07	0.09	0.08	0.02	0.02	1×10^{-3}	1×10^{-7}		

[a] Carrier mobilities calculated in saturation within the charge carrier concentration range of $3-4 \times 10^{12}$ cm^{-2}. Standard deviations are typically <10%; otherwise a mobility range is given. [b] Polymer layer thickness is given by d. [c] From DSC data. [d] These films fabricated directly on Si substrates without a thermal oxide coating.

densities.[66,67] To investigate the universality of the device performance alterations with gate dielectric, representative p- and n-channel organic semiconductors have been studied. The present OTFT results demonstrate for the first time that, independent of the polymer structure, film architecture, and organic semiconductor, the surface T_g of polymer gate dielectrics is invariably lower than that of the bulk. To the best of our knowledge, this is the first report showing reduced polymer film surface T_g's even in the case of attractive substrate interfacial interactions.

Results

Here we present results exploring the correlation between OTFT response properties and polymer film surface T_g effects. Pentacene, a representative, structurally well-characterized p-type organic semiconductor, is first employed since pentacene-based TFTs afford relatively high and constant device performance on c-SiO_2 over a range of deposition temperatures. Investigated polymer dielectric architectures include polymer films having neutral/repulsive substrate interactions (PS, PMS, and PTBS), films having attractive substrate interactions (PMMA and P2VP), multilayer, and plasticizer-doped polymer films. Additional corroborative experiments such as OTFT response as a function of polymer film thickness, surface T_g modification via O_2 plasma treatment, and post-annealing experiments are also presented. Finally, to investigate the universality of OTFT response as a probe of surface T_g, other well-characterized organic semiconductors are also examined, and comparisons to pentacene TFTs are discussed.

OTFT Fabrication and Performance. Top-contact/bottom-gate TFTs were fabricated using spin-coated polymer dielectric films on 300-nm-thick SiO_2 gate substrates (except for 800 nm PS1 films which were fabricated on Si substrates without a thermal oxide coating). Devices were then fabricated on the various polymer gate dielectrics by vacuum-depositing the organic semiconductors (50 nm) at predetermined substrate temperatures T_D, followed by Au source-drain contact deposition. Transfer characteristics of the resulting devices were measured in the saturation regime ($|V_{DS}| \geq |V_G - V_T|$), and representative transfer plots are shown in Figures 4 and S1–S3. Tables 1–2 and S1–S3 collect the OTFT performance parameters, carrier mobility in the saturation regime (μ_{sat}),[68] current on/off ratio (I_{on}/I_{off}), and threshold voltage (V_T). For comparison, μ_{sat} is calculated for all devices at the same charge carrier concentration range of $3-4 \times 10^{12}$ cm^{-2}.

a. Polymer Films Having Neutral or Repulsive Substrate Interactions. Thin polymer films (<100 nm in most cases) having neutral or repulsive substrate interactions exhibit reduced T_g values compared to bulk T_g values as the film thickness is decreased.[12–15,17,19–29] For extensively studied PS films on silicon or silica substrates, the measured T_g values are independent of molecular weight and the data are described by the empirical relation:[12,19,28]

$$T_g(h) = T_g(b)[1 - (A/h)^{\delta}] \quad (1)$$

where $T_g(h)$ is the value of T_g for a film of thickness h, and $T_g(b)$ is the value of T_g for bulk PS. The best fit for the measured T_g values is provided by constants $A = 32$ Å and $\delta = 1.8$ (Figure 3B). Since spectroscopic techniques such as ellipsometry and fluorescence spectroscopy have been used to define this empirical formula, "surface" T_g values for PS films can roughly be extrapolated from eq 1 to ~ -40 °C versus the bulk values.

Pentacene TFTs fabricated on polymer gate dielectrics with neutral or repulsive substrate interactions (PSs, PMS, and PTBS) exhibit typical linear/saturation behavior in $I-V$ transfer and output plots (Figures 4, S1–S2). As shown in Figure 4, PS1-based pentacene devices fabricated at high T_D (>60 °C) afford 2–3 orders of magnitude lower I_{DS} at all gate voltages compared to those fabricated at low T_D, resulting in T_D-dependent device performance. Pentacene devices on other gate dielectrics (PS samples with different molecular weights, PMS, and PTBS) exhibit similar behavior (Figures S1 and S2) to those fabricated on the PS1 gate dielectric.

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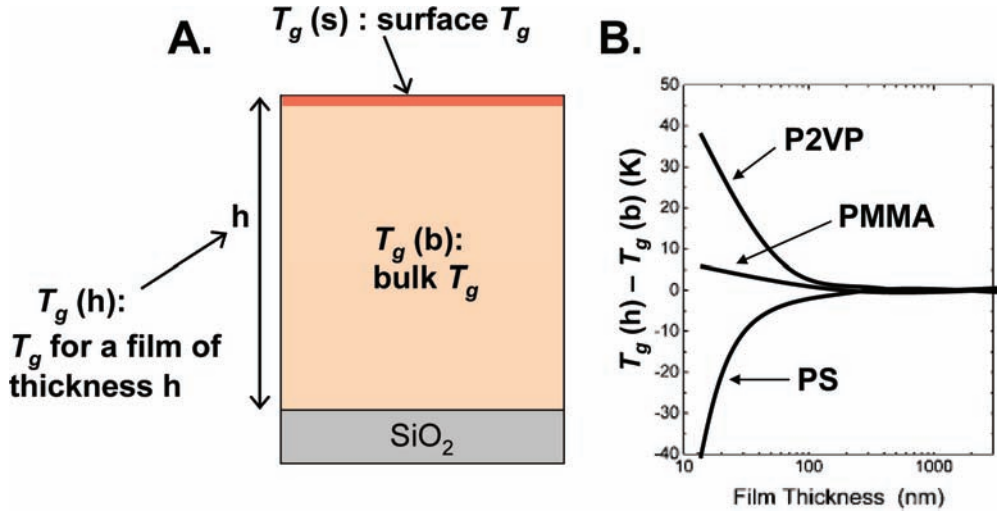

Figure 3. (A) Schematic representation of various polymer film T_g values: T_g(s) (surface T_g), T_g(b) (bulk T_g), and $T_g(h)$ (T_g for a film of thickness h). (B) $T_g(h) - T_g$(b) as a function of film thickness for PS, PMMA, and P2VP films. Solid lines are drawn on the basis of the data in refs 28 (PS), 13 (PMMA), and 16 and 44 (P2VP).

Table 2. Field-Effect Mobility Data (μ_{sat}, $cm^2/V\cdot s$)[a] for Pentacene TFTs Fabricated on Various Polymer/SiO_2 Gate Dielectrics as a Function of Pentacene Film Deposition Temperature (T_D)[b]

gate diel.	T_g[c] (°C)	d (nm)	T_D (°C) 25	45	50	55	60	65	70	75
PS1/P2VP	103	12/12	0.52	0.59	0.47	0.34	0.20	0.04	0.002	0.006
		12/65	0.56	0.45	0.40	0.39	0.19	0.03	0.004	0.006
		12/205	0.44	0.39	0.32	0.31	0.18	0.03	0.004	0.0002
DOP (4 wt %)-doped PS1	103	18	0.41	0.63	0.69	0.50	0.42	0.07	0.03	3×10^{-4}
		80	0.33	0.55	0.55	0.46	0.39	0.09	0.07	0.004

[a] Carrier mobilities calculated in saturation within the charge carrier concentration range of $3-4 \times 10^{12}$ cm^{-2}. Standard deviations are typically <10%. [b] Polymer layer thickness is given by d, and DOP = dioctylphthalate. [c] From DSC data.

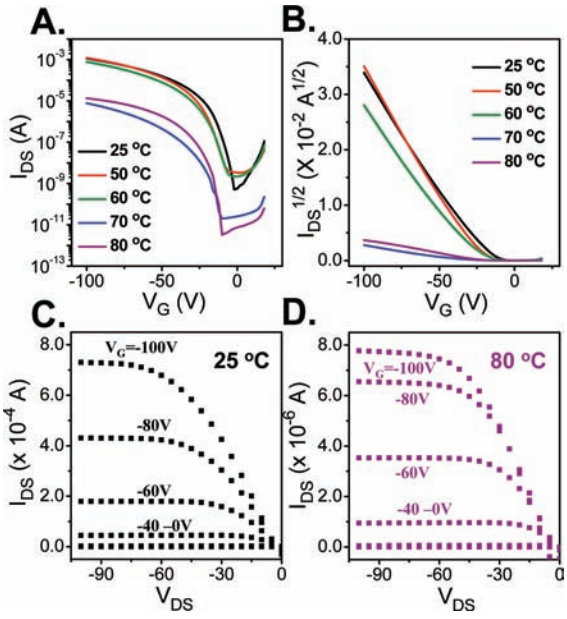

Figure 4. Transfer (A, B) and output (C, D) plots of pentacene TFTs fabricated on PS1 (20 nm) gate dielectric at different pentacene deposition temperature T_D's.

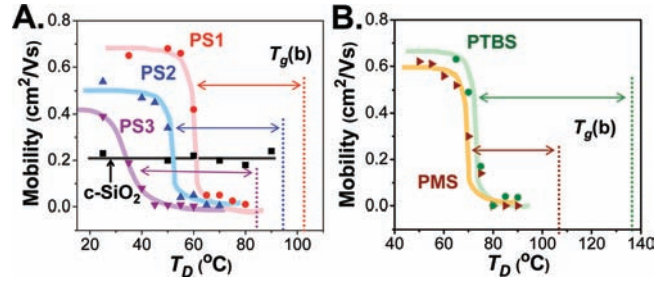

Figure 5. Field-effect mobilities of pentacene TFTs fabricated at the indicated T_D's on the polymer gate dielectrics: (A) PS1 (20 nm), PS2 (24 nm), PS3 (10 nm), and c-SiO_2. (B) PMS (20 nm) and PTBS (30 nm). Dotted and solid lines are drawn as bulk T_g values for each polymer dielectric and as guides to the eye, respectively. Arrows indicate $\Delta T_g(s,b) = T_g(b) - T_g(s)$ differences between surface and bulk T_g values for each polymer dielectric.

The derived saturation field-effect mobility values of pentacene TFTs as a function of polymer gate dielectrics and T_D's are shown in Figure 5 and Table 1. For TFTs based on polymer gate dielectrics, pentacene carrier mobility depends strongly on the T_D's of the specific polymer gate dielectrics. In comparison, pentacene devices on uncoated c-SiO_2 controls afford relatively invariant performance with carrier mobilities of ~0.2 $cm^2/V\cdot s$. For the polymer gate dielectrics, over a narrow and well-defined T_D range, pentacene carrier mobility drops precipitously by >10× from ~0.3−0.7 to $10^{-7}-0.01$ $cm^2/V\cdot s$. This transition temperature is characteristic of the specific polymer gate dielectric and far lower than bulk T_g values of the corresponding polymers measured by temperature-modulated DSC. Here we define this transition temperature as the surface T_g of the polymer film, or T_g(s) (~60 °C for PS1, ~50 °C for PS2, <35 °C for PS3, ~70 °C for PMS, and ~75 °C for PTBS). For the other device performance parameters other than carrier mobility, although increased V_T values are observed at high T_D's for a

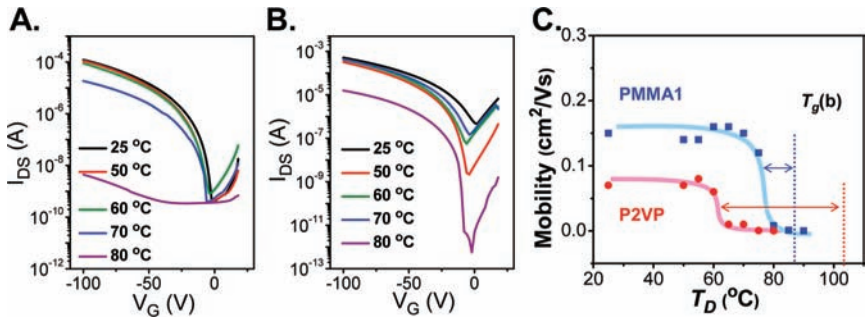

Figure 6. Transfer plots of pentacene TFTs fabricated on (A) P2VP (12 nm) and (B) PMMA1 (20 nm) gate dielectrics at the indicated T_D's. (C) Field-effect mobilities of pentacene TFTs fabricated at the indicated T_D's on PMMA1 (20 nm) and P2VP (12 nm) gate dielectrics. Dotted and solid lines are drawn as bulk T_g values for each polymer dielectric and as guides to the eye, respectively. Arrows indicate $\Delta T_g(s,b) = T_g(b) - T_g(s)$ differences between surface and bulk T_g values for each polymer dielectric.

few cases (e.g., P5 on PS3, Table S1), no clear correlation between V_T values and T_D's are established for all cases (Tables S1−S3, vide infra).

For PSs, devices based on polymer gate dielectrics with higher molecular weights (hence, higher $T_g(b)$) afford higher $T_g(s)$. The temperature difference between surface and bulk T_g values, defined as $\Delta T_g(s,b) = T_g(b) - T_g(s)$, is 40−45 °C, independent of the molecular weight. This demonstrates the molecular weight independence of T_g-nanoconfinement effects, evident here in the narrow range of derived $\Delta T_g(s,b)$ values, and the values of $\Delta T_g(s,b)$ for PSs are in accordance with previous reports, carried out using a variety of experimental spectroscopic techniques.[12,28,35] Similarly, PMS- and PTBS-based pentacene TFTs exhibit well-defined mobility transitions at well-defined temperatures, and $\Delta T_g(s,b)$'s are ∼40 and ∼60 °C, respectively. These values are reasonable considering the reported values in the literature of ∼35 and ∼50 °C, respectively, for 20-nm-thick films.[35]

b. Polymer Films Having Attractive Substrate Interactions. Polymer films having attractive substrate interactions have been reported to exhibit elevated T_g values versus their bulk values as the film thickness is decreased, due to hindered polymer segmental dynamics at the substrate interface. Examples are the strong interactions of PMMA or P2VP repeat units with the surface hydroxyl group of the SiO_2/Si substrate (Figure 1).[16] The P2VP films display a very large increase in T_g with decreasing thickness (∼ +40 °C for 15 nm-thick film),[16,39,44] while the PMMA films exhibit only a slight increase in T_g (∼ +5 °C for 14 nm-thick film; Figure 3B).[13] The T_g increase for PMMA or P2VP films has been explained in terms of the attractive substrate interactions having a greater impact on the T_g than do the relatively small free-surface effects present in the films. However, since this measurement is based on spectroscopic assays of average T_g values across a certain film thickness, the question arises as to whether there will be enhanced polymer segmental dynamics at the free surface of the polymer film, hence reduced T_g's.

Pentacene TFTs were fabricated on PMMA1 and P2VP gate dielectrics at different T_D's. Similar to the devices on polymer films having neutral or repulsive substrate interactions, these devices show typical $I-V$ transfer plots (Figures 6A and B), and the derived saturation field-effect mobility values are shown in Figure 6C and in Table 1. As shown in Figure 6A, P2VP-based pentacene devices fabricated at high T_D values (>70 °C) afford 3−4 orders of magnitude lower I_{DS} at all gate voltages compared to those fabricated at low T_D. Similar T_D-dependent device performance is observed for PMMA1-based pentacene TFTs (Figure 6B). The saturation field-effect mobility values of pentacene TFTs on PMMA1 and P2VP gate dielectrics exhibit a pronounced transition from 0.1−0.2 $cm^2/V\cdot s$ at $T_D < T_g(s)$ to 10^{-7}−0.01 $cm^2/V\cdot s$ at $T_D > T_g(s)$. The estimated $T_g(s)$ values are therefore ∼75 and ∼60 °C for PMMA1 and P2VP films, respectively. Interestingly, for both PMMA1 and P2VP films, the measured $T_g(s)$ values are significantly lower than the $T_g(b)$ values of the corresponding polymers, with $\Delta T_g(s,b)$ values of ∼10 and ∼40 °C, respectively. To the best of our knowledge, this is the first report in which the surface T_g's (reduced T_g values compared to bulk ones) of polymer films having strong substrate interaction have been measured, clearly demonstrating "free-surface effects" at the polymer film surfaces.

c. Multilayer and Plasticizer-Doped Polymer Films. Enhanced or hindered polymer chain dynamics at the air/polymer or polymer/substrate interface are known not to be localized entirely in the interfacial region but to propagate into the film interior with a continuous distribution, as demonstrated by fluorescence spectroscopy.[28] By selectively placing fluorescent dye molecules in the individual polymer layers within polymer multilayer films, Torkelson et al. were able to quantify the T_g values of each polymer layer and to demonstrate that the cooperative segmental mobility of the PS free-surface layer is appreciably hindered by the interfacial region with the underlying polymer layer.[28,39,40] Due to this effect, the thin (12−14 nm) PS films on PMMA or P2VP underlayer have been shown to exhibit T_g values similar to the bulk ($|\Delta T_g(h,b) = T_g(b) - T_g(h)| < 6$ °C).[39] Furthermore, cooperative polymer chain dynamics can be suppressed by adding small-molecule diluents or plasticizers. Thus, plasticizer-doped PS films have been shown by fluorescence spectroscopy to display thickness-independent T_g values ($\Delta T_g(h,b) \approx 0$ K), indicating reduced nanoconfinement effects.[36,37] Although certain polymer film geometries or small molecule additions to the polymer film can affect overall cooperative segmental dynamics, free-surface effects should persist in all cases. Since pentacene device performance is likely only affected by the surface T_g, hence free-surface effects, reduced T_g values are expected in all cases.

Figure 7 and Table 2 show schematic multilayer and plasticizer (DOP)-doped polymer film geometries and saturation field-effect mobility data for devices fabricated on these gate dielectrics. Similar polymer film geometries to those fabricated in the literature[36,39] were selected for direct comparisons. As shown, the transition for field-effect mobility values at different T_D's occurs at ∼60 °C, independent of the polymer film structure and added plasticizer, and similar to those for pentacene devices on bare PS1 gate dielectrics. Note that there is a substantial

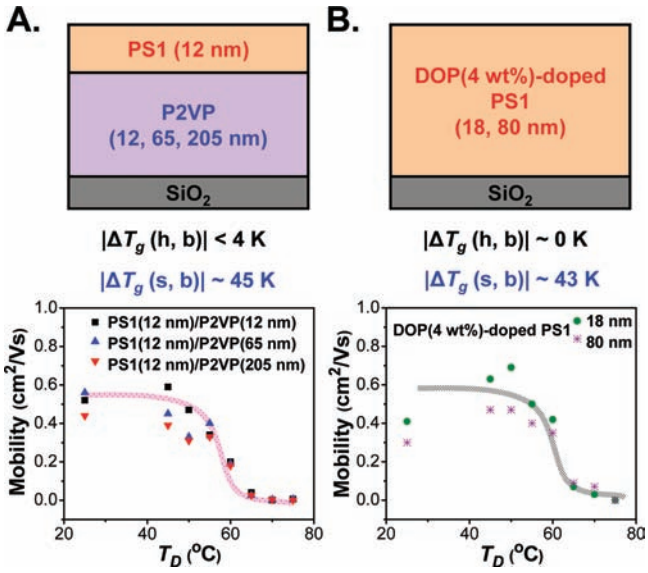

Figure 7. Field-effect mobilities of pentacene TFTs fabricated at the indicated T_Ds on: (A) bilayer polymer dielectrics (PS1/P2VP - 12/12, 12/65, and 12/205 nm), (B) DOP (4 wt %)-doped PS1 gate dielectrics (18 and 80 nm). Solid lines are drawn as guides to the eye. ΔT_g (h,b) values are from refs 39 (multilayer films) and 36 (DOP-doped PS films).

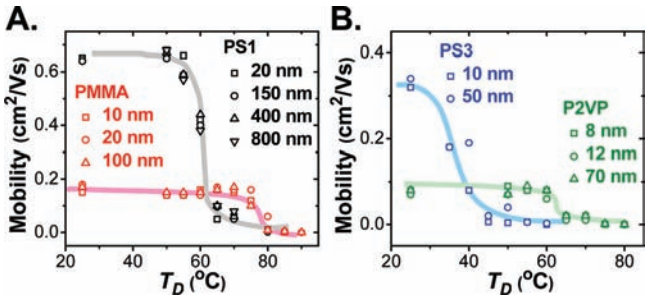

Figure 8. Field-effect mobilities of pentacene TFTs fabricated at the indicated T_D's on polymer dielectrics of (A) PS1 and PMMA1 and (B) PS3 and P2VP as a function of gate dielectric thickness. Solid lines are drawn as guides to the eye.

difference between the ΔT_g(h,b) values reported in the literature[36,39] and ΔT_g(s,b) values derived from this study. This result demonstrates that the free-surface effect at the air/polymer interface is maintained under all conditions, even when the overall cooperative segmental dynamics are altered.

d. Thickness-Independent Surface T_g. That the free-surface effect, hence T_g(s), is a surface and not a bulk polymer property can be demonstrated by analyzing pentacene TFT performance on polymer gate dielectrics as a function of dielectric film thickness. Table 1 and Figure 8 show pentacene carrier mobility values on various polymer gate dielectrics over a wide range of gate dielectric film thicknesses. As shown, for all polymer gate dielectrics, the mobility transition occurs at the same T_g(s) independent of the polymer film thickness, demonstrating the persistence of enhanced polymer chain dynamics at the free surfaces.

e. Modification of Polymer Film Surface T_g. Oxygen-plasma treatment of PS films is known to form oxygenated species (mainly hydroxyl groups) on the polymer surface, penetrating to only a very small depth (~2 nm) into the film.[69,70] Therefore, this treatment should chemically modify the surfaces of the PS films (T_g(b) = 80−100 °C depending on the molecular weight) to approximate those of PVP with a much larger T_g(b) (~170 °C). Pentacene TFTs were then fabricated on the O_2-plasma treated (5 s) PS1 and PS2 gate dielectrics (PS1/2-OXY) at T_D = 70 °C (Figure 9). As a comparison, PS1/2, PVP, and PVP-OXY gate dielectrics were used as a control. The carrier mobilities of the PS1/2-OXY-based devices at $T_D > T_g$(s) for PS1 and PS2 fall in the range of 0.16−0.17 $cm^2/V \cdot s$, much higher than those of the PS1/2-based devices (0.05 $cm^2/V \cdot s$ for PS1 and 0.0004 $cm^2/V \cdot s$ for PS2) despite the low T_g(b)s of these polymers. Indeed, these mobility values approach those of the PVP-based devices fabricated in parallel (~0.30 $cm^2/V \cdot s$). Thus, this result not only demonstrates the surface polymer chain viscoelastic origin of the dramatic mobility variations, but also the practical implications of surface T_g modification.

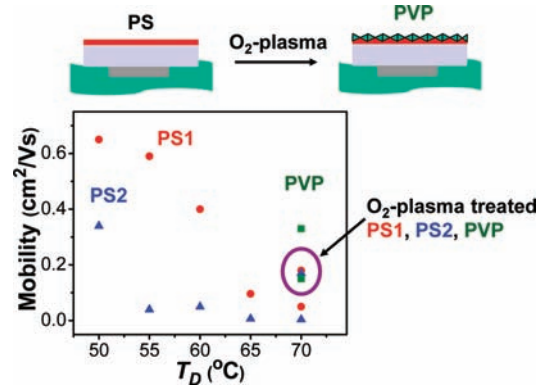

Figure 9. Field-effect mobilities of pentacene TFTs fabricated at the indicated T_D's on different PS1, PS1-OXY, PS2, PS2-OXY, PVP, and PVP-OXY gate dielectrics.

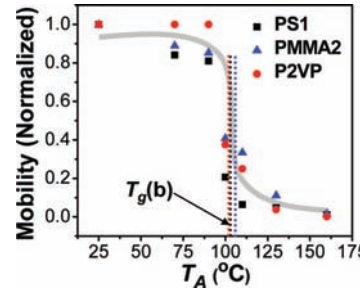

Figure 10. Field-effect mobilities of pentacene TFTs fabricated on PS1 (80 nm), PMMA2 (60 nm), and P2VP (70 nm) gate dielectrics at T_D = 25 °C, followed by post-annealing at the indicated temperatures (T_A = 70−160 °C). Solid lines are drawn as guides to the eye.

f. Post-Annealing of Pentacene Transistors. To demonstrate that pentacene TFT performance variations are solely the consequence of polymer dielectric surface dynamics, polymer film surfaces were modified by depositing pentacene molecules on the various polymer gate dielectrics (PS1, PMMA2, and P2VP) at room temperature (T_D = 25 °C), followed by post-annealing of the fabricated devices under nitrogen on a hot plate for 1 h at preset annealing temperatures, T_A. As shown in Figure 10 and Table S3, the normalized carrier mobility values for these devices exhibit transitions not at $T_A = T_g$(s) but at $T_A = T_g$(b). Since the polymer film surface was covered by pentacene molecules at room temperature in these experiments, thus largely suppressing free surface effects, the polymer segments can only undergo cooperative chain dynamic motions above T_g(b). The

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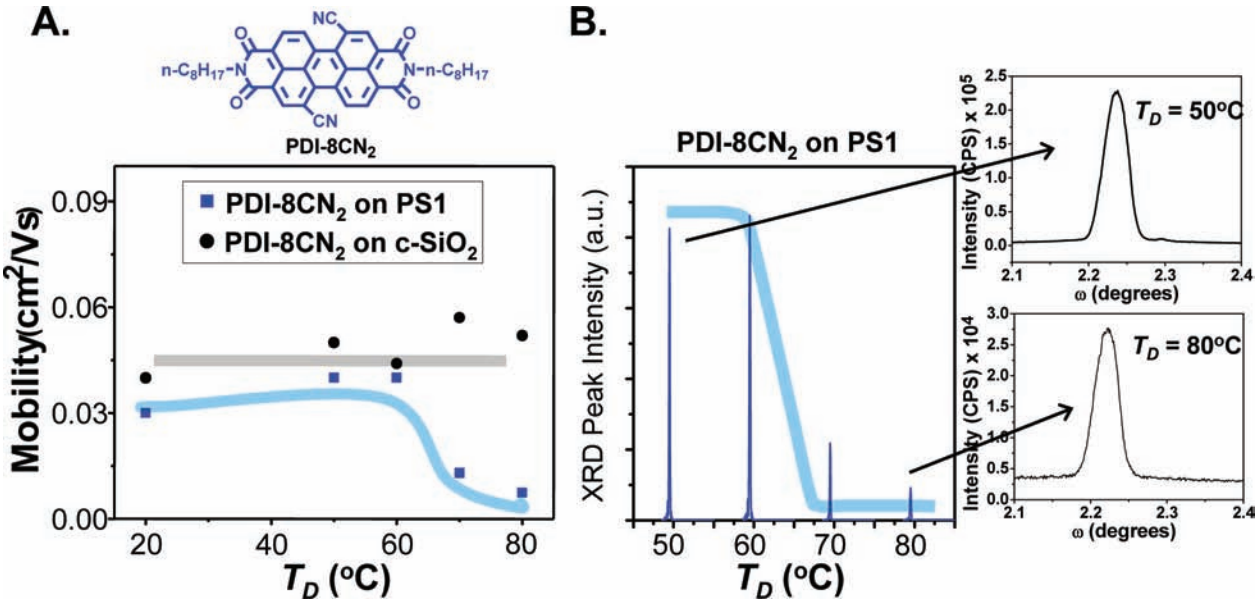

Figure 11. (A) Field-effect mobilities of PDI-8CN$_2$ TFTs fabricated at the indicated T_D's on polymer gate dielectric PS1 (20 nm) and on c-SiO2. (B) XRD ($\theta/2\theta$ and ω scans) data for 50 nm thick PDI-8CN$_2$ films grown on PS1 (20 nm) gate dielectrics at the indicated T_D's. The solid lines are drawn as guides to the eye.

device performance transition at T_g(b) of the polymer gate dielectrics can then be attributed to distortion of the pentacene film texture arising from polymer chain dynamics of the underlying layer, and reevaporation[71,72] of the pentacene films at higher annealing temperatures.

g. Other Organic Semiconductor-Based Transistors. Finally, to investigate the generality of surface T_g measurements via TFT performance, various organic p- (α-6T) and n-type (PDI-8CN$_2$,[73] DFH-4T,[74] DFHCO-4T,[75] and DFO-PTTP[76]) semiconductors were employed for device fabrication on PS1 and c-SiO$_2$ gate dielectrics. Only the n-channel semiconductor PDI-8CN$_2$ shows a similar mobility transition at $T_D = T_g$(s) on PS1 (Figure 11A). With the exception of DFHCO-4T, the other organic semiconductors afford higher field-effect mobilities at higher T_D's, even at $T_D > T_g$(s) (Figure S3), possibly due to enhanced film texturing via annealing at higher temperatures, which is frequently observed for organic semiconductors. The unique characteristics of the P5- and PDI-8CN$_2$-derived TFTs in probing the surface T_g's of polymer films is possibly attributable to the relatively constant and favorable device performance (hence, high film crystallinity) over a range of T_D's observed on conventional SiO$_2$ substrates. Significantly reduced film texturing of PDI-8CN$_2$ films on PS1 at $T_D > T_g$(s) is evident in the XRD data as diminished reflection intensities in $\theta/2\theta$ scans and broadened/noisy rocking curves of the (001) reflection (Figure 11B).[77]

Discussion

Pentacene Microstructure and Growth Mode Variation. The origin of the strong dependence of pentacene TFT carrier mobility on polymer dielectric surface viscoelastic properties, hence surface T_g, is investigated here via pentacene film microstructure and transport properties as influenced by growth on the various polymer gate dielectrics. Thin-film X-ray diffraction (XRD) and atomic force microscopy (AFM) data are crucial for evaluating polycrystalline vacuum-deposited organic thin films in terms of texture/ordering and growth mode (grain size), respectively, both of which are often correlated with the field-effect mobility. The vacuum-deposited pentacene films (1.5, 2.5, 5, and 50 nm thick) grown at different T_D's were studied by XRD ($\theta/2\theta$ and ω scans) and AFM. Figure 12 shows $\theta/2\theta$ XRD scans and rocking curves (ω scans) of 50 nm thick pentacene films grown on various polymer gate dielectrics (PS1, PMMA1, and P2VP) and on a c-SiO$_2$ substrate at different T_D's. Vacuum-deposited pentacene films exhibit two characteristic polymorphs, the "thin-film" and "bulk" phases with *d*-spacings of 15.4 and 14.5 Å, respectively.[78,79] The thin-film phase is known to be a metastable polymorph,[80] which is irreversibly converted to the more stable bulk phase by either annealing[81] or solvent treatment.[82] Most of the pentacene films employed in this study exhibit only the thin-film phase due to small film thicknesses and the relatively fast growth rates, with the (001) Bragg reflection ($2\theta = 5.74°$) intensity showing a pronounced dependence on T_D.[79] Similar behavior is observed for pentacene devices fabricated on PS1/P2VP (12/12 nm) and DOP-doped PS1 (18 nm) gate dielectrics (Figure S4). Pentacene films (50 nm) grown at low deposition temperatures ($T_D < T_g$(s)) exhibit 1−2 orders of magnitude greater (001) peak intensities compared to films grown at high deposition temperatures. In comparison, note that 50 nm pentacene films grown on c-SiO$_2$ substrates

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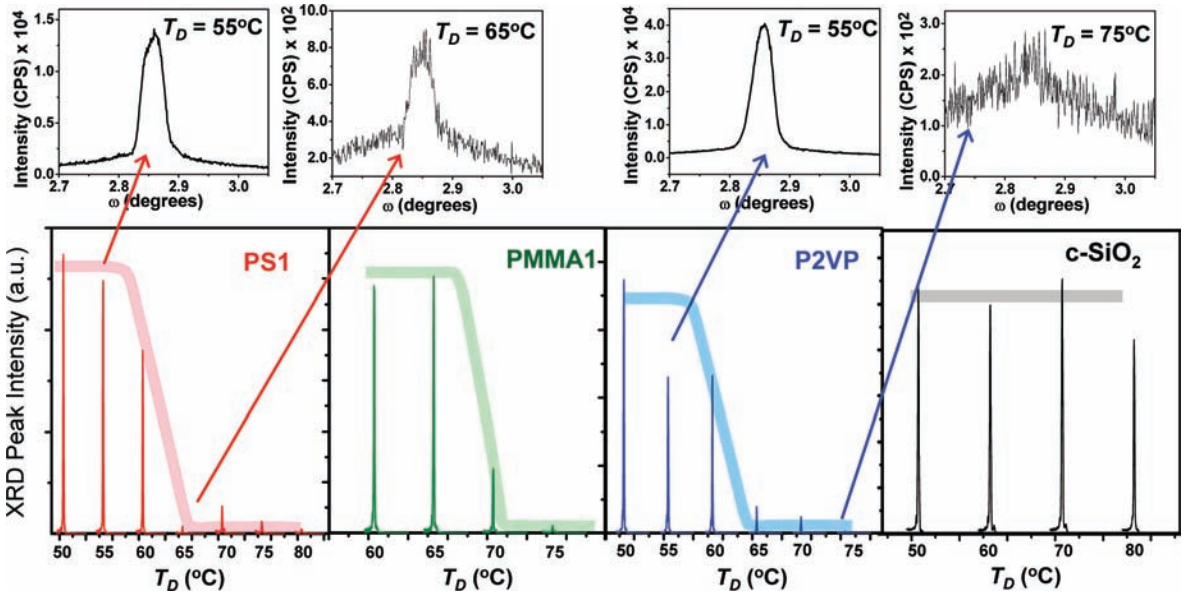

Figure 12. XRD ($\theta/2\theta$ and ω scans) data for 50-nm-thick pentacene films grown on PS1, PMMA1, P2VP, and c-SiO2 gate dielectrics at the indicated T_D's. The solid lines are drawn as guides to the eye.

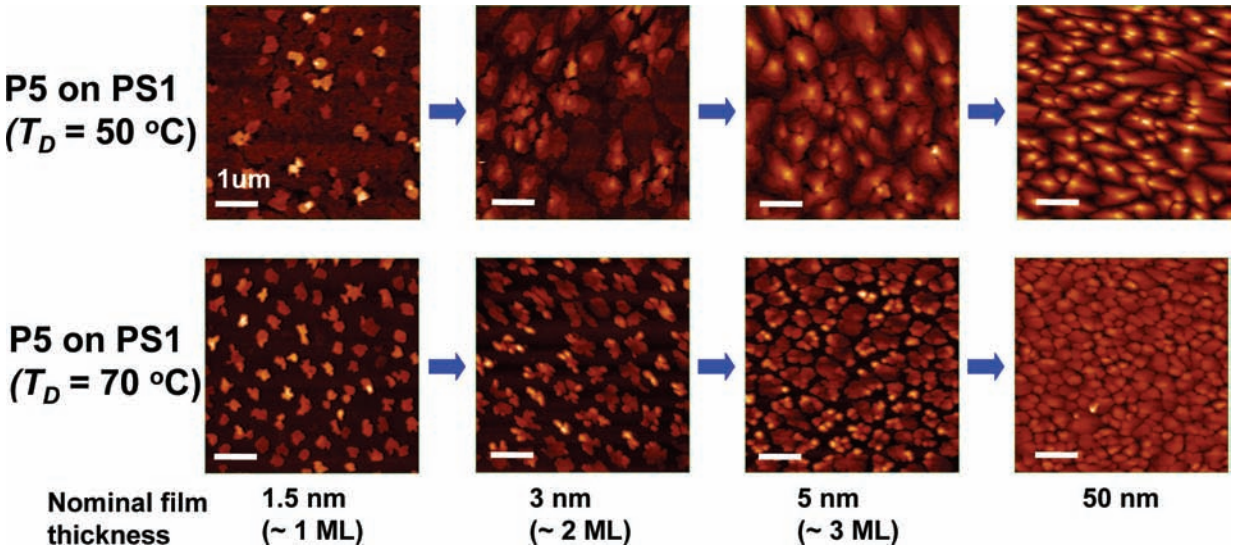

Figure 13. AFM images (5.0 × 5.0 μm^2) of vacuum-deposited pentacene films (1.5−50 nm) grown on PS1 gate dielectrics at the indicated T_D's. The scale bars indicate 1 μm.

exhibit relatively invariant (001) peak intensities over a wide range of T_D. Details of pentacene film out-of-plane texturing were studied via the rocking curves of the first-order reflections for selected samples at specific T_D's, focusing especially on the full-width-at-half-maximum (fwhm) values. As shown in Figure 12, rocking curves of the pentacene film (001) reflection on polymer gate dielectrics at $T_D > T_g$(s) are more ill-defined and less intense versus those of films grown at lower deposition temperatures. Furthermore, pentacene films grown at high T_D's afford relatively large fwhm values (>0.05°; difficult to define in some cases) in the rocking curves versus those grown at low T_D's (fwhm ≈ 0.03°), indicating significantly less texturing. These results demonstrate that enhanced polymer segmental movement at the free surface of the polymer gate dielectrics with increasing T_D strongly disturbs the growth of highly textured pentacene films, resulting in far lower film crystalline texturing.

Pentacene film growth mode monitoring by AFM images reveals similar transitions near T_g(s), with the films grown on polymer gate dielectrics exhibiting very different behavior from those on c-SiO_2. Figures 13 and S5 show AFM images of pentacene films (1.5, 3, 5, and 50 nm) grown at T_D = 50 and 70 °C on PS1 and c-SiO_2, respectively. Pentacene molecules deposited on PS1 at T_D = 50 °C < T_g(s) grow in a layer-by-layer mode, resulting in almost complete first monolayer coverage before the next layer grows. This results in relatively large grains for the 50 nm thick films. For pentacene deposition at T_D = 70 °C > T_g(s), the relatively large number of nucleation sites affords an island growth mode, forming small grains for the 50 nm thick films (Figure 13).[83] In marked contrast, pentacene films grown on c-SiO_2 afford layer-by-layer growth

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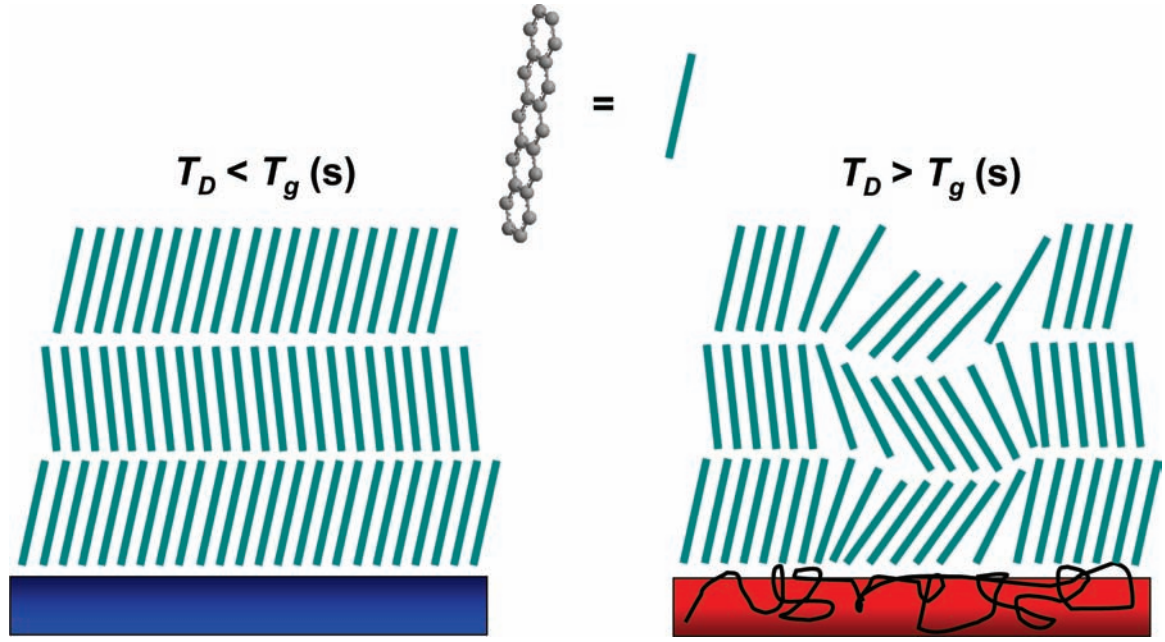

Figure 14. Schematic diagram of pentacene film microstructural variation on polymer gate dielectrics at different T_D's.

mode at all T_D's, affording large grain sizes for 50 nm thick films (Figure S5).

Grain size analysis for the 50 nm thick pentacene films grown on the other gate dielectrics examined in this study reveals a similar behavior. Figures S6 and S7 show AFM images of 50 nm thick pentacene films grown at different T_D's on PS1 and c-SiO_2, respectively. Pentacene films grow with relatively large (>0.8 μm) grain sizes on the c-SiO_2 substrates at all T_D's (Figure S6), with monotonic increments in size when T_D is increased from 25 to 80 °C, due to increased molecular diffusion at these higher temperatures.[84,85] However, for pentacene films grown on PS1, the grain size increases slightly for $T_D < T_g$(s) [~1.2 μm at $T_D = 25$ °C to ~1.4 μm at $T_D = 60$ °C], then abruptly decreases to <0.5 μm for $T_D > T_g$(s) (Figure S7). Similar behavior is observed for the other glassy polymer gate dielectrics (P2VP, PMMA, and PTBS; Figures S8−S10). Pentacene films grown at high T_D display either relatively small grain sizes or form polycrystalline aggregates separated by large gaps.

The correlation between the pentacene film morphology variations at different T_Ds and film microstructural variations at T_g(s) for these polymer gate dielectrics can be qualitatively understood in terms of the pentacene growth mechanism on different substrates (Figure 14). For c-SiO_2 substrates or polymer gate dielectrics at $T_D < T_g$(s), increasing T_D results in increased grain size due to layer-by-layer film growth arising from enhanced molecular diffusion on the substrate surface.[83−85] The absolute pentacene grain sizes can differ, depending on the substrate and due to differing molecule−molecule vs molecule−substrate interactions, as shown in the AFM images of Figures S6−S10. For polymer gate dielectrics at $T_D > T_g$(s), the pentacene grain size and film texture abruptly fall, possibly due to enhanced polymer surface roughness and/or friction at higher temperatures.[86,87] Rough gate dielectric surfaces are known to disrupt pentacene molecular diffusion, as well as ordered nucleation and growth of highly textured pentacene films, affording smaller grain sizes and low XRD peak intensities.[78,88,89] This can be readily seen in the initial pentacene film growth stages (~5 nm) on PS1 gate dielectrics as a function of T_D (Figure S11). Since pentacene film texture and grain boundaries are correlated with TFT device performance,[43,78,88] the transition in pentacene film morphology, microstructure, and device carrier mobility occurs at the same temperature T_g(s).

Conclusions

In this study, we demonstrate how the surface viscoelastic properties of glassy polymer gate dielectrics affect organic semiconductor film growth, microstructure, and OTFT response characteristics. On the basis of a variety of glassy polymer dielectric architectures and geometries employed in this study, we have shown that transitions from high (0.1−0.7 $cm^2/V \cdot s$) to low ($0.01-10^{-7}$ $cm^2/V \cdot s$) carrier mobilities occur at well-defined organic semiconductor film growth temperatures, characteristic of each top polymer layer of the bilayer gate dielectric. This temperature, defined herein as T_g(s), is significantly lower than T_g(b) and completely film thickness independent. Furthermore, the transition from high to low carrier mobility is inextricably correlated with dramatic microstructural and morphological alterations of the semiconductor film occurring at the same T_g(s). Finally, the way in which T_g(s) is defined and quantified here, via field-effect transport measurements, represents a unique new and sensitive technique to probe polymer surface thermal/viscoelastic properties vs those of thin-film and bulk regions. As a concluding remark, we believe that this study broadens our understanding of film growth and TFT response and will contribute significantly to the development of organic semiconductor/polymer-based electronics.

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Supporting Information Available: Experimental Section, AFM image, XRD, and OTFT device performance data for chosen dielectric materials. This material is available free of charge via the Internet at http://pubs.acs.org.

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